

Applicant: Cheng-Liang Hou

Examiner: Jain, Raj K.

Serial No.: 10/694,732

Group Art Unit: 2651

Filed: October 29, 2003

Docket No.: 0063-115001/BU3130

Title: SYSTEM AND METHOD FOR VARIABLE DATA TRANSMISSION RATE RESOLUTION

REMARKS

Applicant has reviewed the final Office action mailed November 18, 2008. This response is filed with Request for Continued Examination and a petition for a two-month extension of time and because April 18, 2009, fell on a Saturday this response therefore is timely.

Claims 1-4, 6-12, 14-19, and 21-22 are pending. Claims 1-4, 6-12, 14-19, and 21-22 have been amended. Claims 5, 13, and 20 have been cancelled. Claims 1, 9, and 16 are independent.

Claims 1, 2, 5-6, 8-10, 13, 15-17, 20-21 were rejected as allegedly anticipated by Marin (US Patent No. 5,936,940). Applicants respectfully request withdrawal of this rejection because Marin fails to disclose all the elements of independent claims 1, 9, and 16.

Claim 1 recites a method that includes storing first and second pluralities of data transmission rates in a register, wherein each of the first plurality of data transmission rates are spaced from each other by a first incremental value and wherein each of the second plurality of data transmission rates are spaced from each other by a second incremental value greater than the first incremental value. A request to transmit data over a port of a switch at a requested transmission rate is received. One of the first plurality of data transmission rates or one of the second data transmission rates is selected at which to transmit data over the port, where the selected transmission rate is based on the requested transmission rate, and data is transmitted through the port using the selected data transmission rate.

Marin does not disclose, for example, “storing a first plurality of data transmission rates in a register” or “storing a second plurality of data transmission rates in a register.” In contrast, Marin indicates that transmission rates are calculated and stored in tables. A person of skill in the art would understand that tables are logical constructs that generally are stored in RAM memory and which are quite different from registers. Using a very limited number of registers, as in claim 1, reduces the chip cost, as explained in, e.g., ¶¶ 0004 – 0007 of the application.

Marin also does not disclose a “storing a first plurality of data transmission rates in a register, wherein each of the first plurality of data transmission rates are spaced from each other by a first incremental value” and “storing a second plurality of data transmission rates in a register, wherein each of the second plurality of data transmission rates are spaced from each other by a second incremental value greater than the first incremental value.” Instead, Marin

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discloses calculating a plurality of values that have a spacing that varies between each of the consecutive values. See, e.g., col. 9:34 – col. 10: 30.

Thus, claim 1 is allowable at least of the above reasons. Claims 2-4 and 6-8 depend from claim 1 and are allowable at least for the same reasons claim 1 is allowable. Claims 9 and 16, and their dependent claims, contain similar subject matter to that of claim 1 and are allowable at least of the same reasons claim 1 is allowable.

Conclusion

Applicant believes that all the application is condition for examination on the merits and respectfully requests such examination. The Examiner may telephone Applicant's attorney (202-470-6453) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

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Date April 20, 2009

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